An Integrated System for Simultaneous, Multichannel Neuronal Stimulation and Recording

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***Abstract*—Precision electronics that provide multi-electrode stimulation and recording capabilities are an important tool for the experimental study of neuronal development and plasticity. Towards this end, we present a custom analog integrated circuit (IC), fabricated in a 0.35-μm process, incorporating stimulation buffers and recording preamplifiers for multiple electrodes onto a single die. The architecture of the IC allows for arbitrary, independent configuration of electrodes for stimulation or recording, and the IC includes artifact-elimination circuitry that returns the stimulation electrode to its previous voltage following stimulation, minimizing the interference with recording. We analyze the thermal noise levels in the recording preamplifiers and experimentally measure input-referred noise as low as 4.77 $\mu\mathrm{V_{rms}}$ in the frequency range of 30 Hz–3 kHz at a power consumption of 100 μW from a total power supply of 3.8 V. We also consider the temporal response and stability of the artifact elimination circuitry. We demonstrate that the use of the artifact-elimination circuitry with a 30-μm diameter stimulation electrode permits a return to recording mode in $\leq$ 2 ms after stimulation, facilitating near-simultaneous stimulation and recording of neuronal signals. (Patent applied for, U.S. No. 2007/0178579.)**

***Index Terms*—Analog VLSI, multi-electrode array (MEA), neural stimulation and recording, stimulation artifact.**

I. Introduction

BIOLOGICAL neuronal networks encode information through the transfer of ions across the cell membranes, making biological neural processing an electrical phenomenon and suggesting that electronic interfaces to biology can be important components of experimental systems to study neuronal development and plasticity. Combined with electrodes, which are necessary to transduce biological ionic currents into electronic currents, an electronic interfacing system permits both observation of the electrical activity inherent to neuronal information processing and the application of artificially generated electrical signals that modify the neuronal activity [1], [2]. The design of the electronics capable of both stimulation and recording requires careful consideration of many issues common to analog design (noise levels, stability, and filtering topologies), as well as some unique to neuronal interfacing (simultaneous stimulation and recording).

Experimenters often use electrodes that are part of a multi-electrode array (MEA), or a microfabricated grid of electrodes, because of their advantages of high spatial resolution and chronic biocompatibility [1], [3]. The first advantage, spatial resolution, is inherent to MEA fabrication, which relies on the same microscale technologies used in very large scale integration (VLSI) technology, such as photolithography and etching. Just as in the fabrication of integrated circuits (ICs) or printed circuit boards, the manufacturing and processing of MEAs results in dimensions on the order of microns. The second advantage, chronic biocompatibility, is a result of the use of extracellular electrodes. Unlike intracellular electrodes, which injure cells by puncturing the cell membrane, extracellular electrodes minimize cell damage by measuring the electrical signals present in the extracellular medium. Combining the use of extracellular electrodes with proper control of the neuronal tissue through maintenance of the extracellular environment can extend cell survival for over a year, allowing for very long term experiments [4]. Neuroscientists rely on the advantages of MEAs in many studies of neuronal development and plasticity [5], [6].

Unfortunately, MEAs provide poor coupling of neuronal signals to the electronics. The extracellular electrodes do not measure membrane potentials directly; rather, they record the electric field induced by ionic channel currents [7], [8]. This electric field decreases with distance from the cell, so that the voltages present at the electrode are in the microvolt range, even though membrane potentials are in the millivolt range [1]. Because of the small magnitudes of the extracellular signals, the electronics must provide large amplification while introducing minimal noise. Often, amplification systems are assembled from standard, readily available analog components, such as instrumentation amplifiers. This approach is suitable for small arrays; however, difficulties in system assembly arise as large MEAs require large numbers of components. This difficulty in interfacing drives the development of VLSI systems for amplifying and recording signals from MEAs [9], [10].

Recording alone is insufficient to investigate neuronal behavior or the development of neural connectivity because many applications also require electrical input to the neural culture. Ideally, the experimenter should have the capability to switch the functionality of any electrode between stimulation and recording [11], [12]; however, an effect known as the stimulation artifact interferes with such flexibility by causing localized interference with recording for hundreds of milliseconds after stimulation. This effect is a result of the

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large disparity in magnitude between extracellular signals and stimulation signals at the electrode. As previously noted, signal losses in extracellular interfacing limit recorded signals to the microvolt range. This same attenuation occurs in reverse, from the electrode to the neuronal tissue, so that only a fraction of the applied stimulation voltage reaches the neurons. In order to cause sufficient membrane depolarization sufficient to evoke activity, the electronics must apply stimulation signals in the range of one volt. These large stimulation voltages present at the electrode saturate or distort the sensitive recording system. During the duration of the stimulation artifact, recording cellular activity is impossible.

Literature and commercial systems present methods for stimulation and recording without interference from stimulation artifacts, usually at the expense of functionality. In the simplest method, the experimenter must designate electrodes as stimulation or recording sites for the duration of the experiment, thus sidestepping the problem of recording at the site of the largest artifacts. Often, electronics designers place sample-and-hold (S/H) circuitry at the input of the recording amplifier to prevent saturation of the electronic system during stimulation [2], [13]. Another common technique is to blank, or disable, recording amplifiers near stimulation sites for up to 10 ms after stimulation [14]. Many techniques focus on post-processing to filter out stimulation artifacts from neighboring electrodes [15], [16]. These approaches all concede the data closest to the stimulation, both temporally and spatially, as lost to the stimulation artifact; however, these data may represent the most significant response to the stimulation.

An alternative approach to reducing the interference from the stimulation artifact is to return the stimulation electrode to its pre-stimulation voltage (kept in a S/H) immediately after stimulation [17]. This method provides an effective stimulation while minimizing the artifact, both at neighboring electrodes and at the stimulation electrode. A possible difficulty with this system is that, should neuronal activity occur immediately before the start of a stimulation, the S/H would store a voltage that does not correspond to the actual electrode offset. Also, the area and power requirements render the design unsuitable for VLSI technology—an important requirement as the natural scalability of VLSI systems keeps pace with growing sizes of MEAs.

In this paper, we present a VLSI design for multi-electrode, near-simultaneous stimulation and recording circuitry. The IC provides an interface between biology and a data acquisition system (Fig. 1). To conserve die area, we use simple amplifier stages as the building blocks of the design. Further area conservation results from dual use of the feedforward amplifier for recording and artifact elimination.

II. Design

In the course of experimental use, the electronic system must perform three major functions: recording, stimulation, and artifact-elimination. We consider the functional requirements of each, and we present and analyze the design of an IC implementation of the desired functionality.

A. Design Requirements

Because the electrodes provide the connection between the biology and electronics, their structure greatly influences the performance of many aspects of our design; thus, we must consider the properties of the electrodes that we will use. An important property of an electrode is its impedance. The use of high impedance electrodes provides neuroscientists with the ability to localize small signal sources [18]. Low impedance electrodes, however, introduce less thermal noise into the recordings, according to

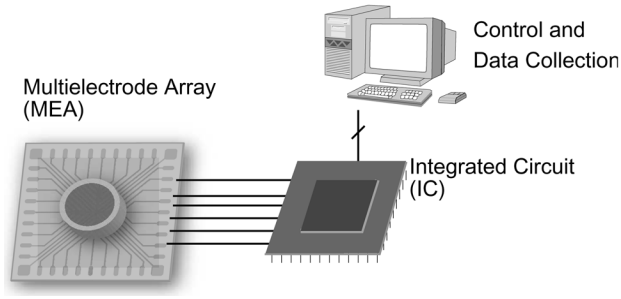

Fig. 1. Diagram of the complete biological interfacing system, including the MEA, IC, and computer interface. The IC contains an array of 16 stimulation and recording elements, each matching with an electrode.

$$\overline{v^2_{\mathrm{noise,elec}}} = 4kT\Re(Z)\Delta f \tag{1}$$

where k is the Boltzmann constant, T is the absolute temperature, $\Re(Z)$ is the real part of the electrode impedance, and Δf is the frequency bandwidth over which measurements are made [19]. Commercial electrodes strike a balance between these extremes in impedance, typically having impedance magnitudes in the range of 100 kΩ to 1 MΩ at 1 kHz. Although extracellular electrodes are complex electrochemical systems with nonlinear dynamics, approximation as a linear capacitor in series with a linear resistor suffices in many cases [20], [21]. Under the assumption that the impedance is primarily capacitive, these typical impedances correspond to capacitances of 1.6–16 nF. For high frequencies, the spreading resistance (due to the resistivity of the extracellular medium), typically 5–100 kΩ, dominates over the electrode capacitance.

Recording consists of faithfully amplifying the small neuronal signals present at the electrodes while rejecting unwanted interference. The noise floor of the recording preamplifiers limits the ability to detect action potentials. Extracellularly recorded action potentials typically have maximum amplitudes $\leq$ 100 μV and frequency components in the range of 30 Hz–3 kHz, requiring input noise $\ll$ 20 $\mu\mathrm{V_{rms}}$ in that bandwidth. Additionally, the preamplifier must reject the low frequency offsets inherent to electrodes. These electrochemical offsets, which can be as large as 100 mV, can saturate the recording preamplifiers. Traditional ac coupling effectively blocks dc offsets to prevent saturation, but requires large capacitors that are not suitable for monolithic integration. We use a mixture of active circuitry and small value capacitors to block low frequency components.

Stimulation requires the application of signals of sufficient magnitude to evoke neuronal activity while minimizing electrochemical damage to the electrodes. Compliance limits on the stimulation voltage serve to protect the electrodes. Within these

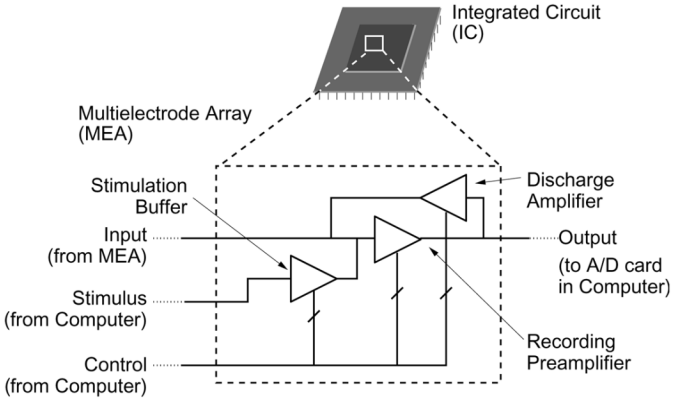

Fig. 2. IC contains an array of 16 stimulation, recording, and artifact-elimination elements, each matching with an electrode.

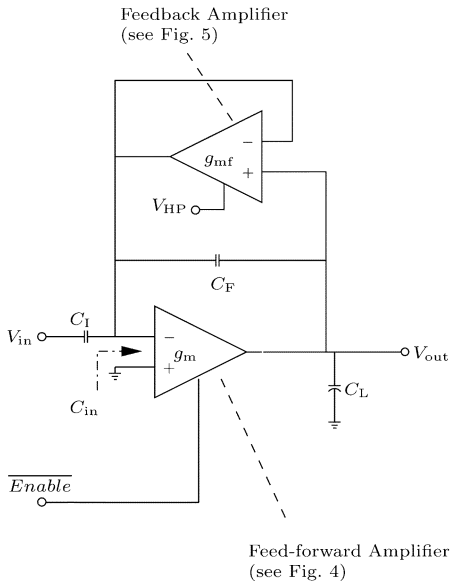

Fig. 3. Topology of the recording preamplifier. Capacitive feedback around the feedforward amplifier sets the recording gain. The enable line of the feedforward amplifier allows disabling during stimulation as part of the artifact-elimination protocol. The feedback amplifier provides a dc pathway to the internal node of the capacitive divider, as well as an adjustable high pass filter to reject electrode offsets.

electrochemical safety limits, many different stimulation protocols are possible, although most protocols fall into two broad categories: voltage control and current control. Literature suggests that voltage control, as a positive pulse followed by a negative pulse, is the most effective method for producing an evoked response [22]. To achieve effective stimulation without electrode damage, we design a current-limited, voltage-output stimulation buffer.

Our final design requirement is that stimulation interfere minimally with recording, both at the stimulation electrode and at other electrodes. Discharging the stimulation electrode to its pre-stimulation voltage is an effective method of eliminating the stimulation artifact. Previously reported systems use separate S/H elements to store the pre-stimulation voltage; however, integrated S/H elements require a large die area and introduce errors due to charge injection [23]–[25]. We present a topology that, by reusing the charge stored in the capacitors of the recording preamplifier, eliminates the need for a separate S/H element [26]. This topology offers the benefits of reduced area and the prevention of additional offsets in the recording path.

B. Design Analysis

The integrated circuit comprises the link between the biological tissue on the MEA and the control and storage capabilities of computer systems. The IC contains an array of identical electrode interface channels, each containing stimulation buffers, recording preamplifiers, and artifact-elimination electronics (Fig. 2). Grouping all the circuitry for one electrode together allows easy expansion of the IC for MEAs with larger electrode counts. Digital circuitry, including shift registers and multiplexers, enables the computer to apply independent control signals to each channel, allowing for independent stimulation and recording on all channels.

1) Recording Preamplifiers: The recording preamplifier uses capacitive feedback to set a gain of $-C_{\mathrm{I}}/C_{\mathrm{F}}$, as Fig. 3 shows. We design for an inverting gain of 50 (34.0 dB) using $C_{\mathrm{F}} = 40$ fF and $C_{\mathrm{I}} = 2.0$ pF. The choice of the closed-loop voltage gain is a compromise between maximizing the output signal level, conserving die area, and stability (see Section II-B–3). Purely capacitive feedback would leave the inverting input of the feedforward amplifier floating, so we must introduce a dc path to that node. A weakly biased transconductance amplifier in the feedback path establishes the dc current path necessary to bias the input. The feedback amplifier also creates a high pass filter that serves to reject the electrode offset voltage. Varying the bias current of the feedback amplifier tunes the high pass cutoff frequency of the recording system. Although the poles of the transfer function are complex, we may make a close approximation with real poles

$$p_{\mathrm{HP}} \approx -\frac{g_{\mathrm{mf}}}{C_{\mathrm{F}}} \tag{2}$$

$$p_{\mathrm{LP}} \approx -\frac{g_m}{C_{\mathrm{I}}}\frac{C_{\mathrm{F}}}{C_{\mathrm{I}}+C_{\mathrm{F}}+C_{\mathrm{in}}} \tag{3}$$

where g_m is the transconductance of the feedforward amplifier, g_{mf} is the transconductance of the feedback amplifier, C_{I} is the input capacitor, C_{F} is the feedback capacitor, and C_{in} is the parasitic input capacitance to the feedforward amplifier. In addition to the two left half plane poles, the bandpass response implies a zero at the origin. There is an additional right half plane (RHP) zero due to the parallel combination of the capacitive feedthrough path and the feedforward amplifier

$$z_{\mathrm{RHP}} = \frac{g_m}{C_{\mathrm{F}}}. \tag{4}$$

This zero is at a very high frequency, so it has only a minor effect on the dynamics of the system.

The feedforward recording amplifier topology (see Fig. 4) is that of a wide range amplifier [27]. Sizing the transistors to

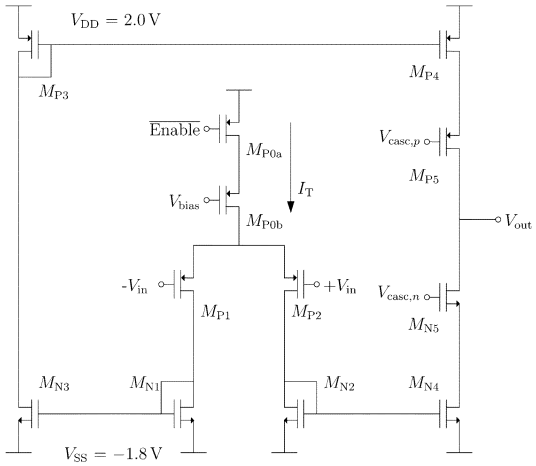

Fig. 4. Feedforward amplifier in the recording system.

TABLE I
TRANSISTOR SIZES AND INVERSION MODES IN THE RECORDING SYSTEM

Transistor	Width (μm)	Length (μm)	Inversion
Feed-forward Amplifier			
M_{P0a}	21.8	3.0	Strong
M_{P0b}	5.0	5.0	Strong
M_{P1}, M_{P2}	200.0	1.0	Moderate
M_{P3}, M_{P3}	4.0	3.2	Strong
M_{P5}	18.0	0.8	Strong
M_{N1}, M_{N2}, M_{N3}, M_{N4}	3.0	11.2	Strong
M_{N5}	6.0	0.8	Strong
Feedback Amplifier			
M_{P6}, M_{P7}	2.0	5.0	Weak
M_{P8}, M_{P9}	2.0	1.0	Weak
M_{N6}, M_{N7}	1.0	20.0	Weak
M_{N8}	10.0	1.0	Weak
M_{N9}	1.0	4.0	Weak

ensure that the input differential pair operates in moderate inversion and the load current mirrors operate in strong inversion (see Table I), such that the input stage transconductance is much greater than the transconductance of any of the current mirror transistors, minimizes the noise contributions of the current mirror transistors, resulting in noise levels near the theoretical limit for a given power dissipation [28]. Neglecting the noise contributions from the current mirror transistors, the midband thermal noise contribution to the output of the recording preamplifier is

$$\overline{v_{\rm no}^2} = \left(1 + \frac{C_{\rm I}}{C_{\rm F}}\right)^2 \frac{16kT}{3g_m}\Delta f. \tag{5}$$

At a bias level of $I_{\rm T} = 13\ \mu{\rm A}, g_m \approx 130\ \mu{\rm S}$, resulting in an input-referred noise of $13\ {\rm nV_{rms}}/\sqrt{\rm Hz}$, or $720\ {\rm nV_{rms}}$ in a 3-kHz bandwidth.

The feedback amplifier (see Fig. 5) uses an operational transconductance amplifier (OTA) topology. Previous implementations of capacitively coupled amplifiers have used a metal-oxide-semiconductor (MOSFET) adaptive element to provide the dc feedback pathway [28]–[30]. Such a topology is effective for normal recording operation; however, the conductance of such an element becomes very large for even a small applied voltage. As we show in Section II-B.3, our

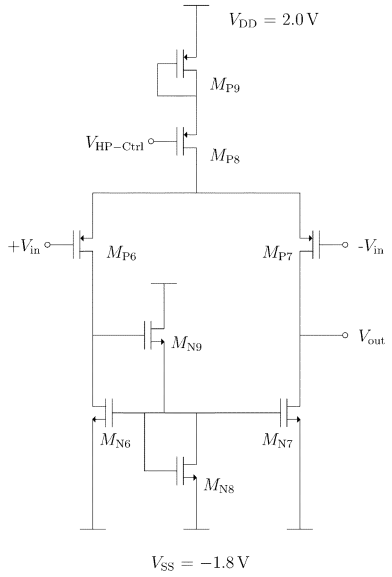

Fig. 5. Feedback amplifier that provides the dc feedback around the feedforward amplifier. $M_{\rm N8}$ and $M_{\rm N9}$ ensure that $V_{\rm ds}$ of $M_{\rm N6}$ is large enough for operation in subthreshold saturation.

artifact-elimination method relies on the charge at the inverting input remaining constant during stimulation; thus, we are unable to use a feedback element that acts as a low impedance path, as it would dissipate the stored charge.

Due to the very small current levels necessary to provide large equivalent resistance values, modifications to the standard OTA topology are necessary. If we had used a standard active load, the didode-connected input transistor $M_{\rm N6}$ would have been in subthreshold triode operation because it would have had its drain-to-source voltage $V_{\rm DS} < 4U_{\rm T}$, where $U_{\rm T}$ is the thermal voltage ($U_{\rm T} \equiv (kT/q)$, where q is the charge of an electron). Two additional transistors $M_{\rm N8}$ and $M_{\rm N9}$ increase the drain-to-source voltage for $M_{\rm N6}$. The diode-connected transistor $M_{\rm N8}$ sinks current that $M_{\rm N9}$ must source. To provide that current, the gate voltage of $M_{\rm N9}$ must rise, increasing $V_{\rm DS}$ of $M_{\rm N6}$. The extra transistor in the tail current bias $M_{\rm P9}$ acts to scale down the bias current relative to the reference current, providing finer control of the high pass cutoff frequency than would be possible with a standard current mirror.

The feedback amplifier has a significant impact on the noise level of the overall amplifier structure. Assuming all transistors in the signal path operate in weak inversion (a safe assumption given the extremely small bias currents necessary), the feedback amplifier produces noise according to

$$\overline{v_{\rm n,fb}^2} = \frac{32kT}{3g_{\rm mf}}\Delta f \tag{6}$$

which is larger than that of an ideal resistive element by a factor of 8/3. The feedback capacitors filter this noise, so that the output noise contribution of the feedback amplifier is

$$\overline{v^2}_{\rm no,fb} = \left(\frac{1}{1 + \frac{2\pi f C_{\rm F}}{g_{\rm mf}}}\right)^2 \frac{32kT}{3g_{\rm mf}}\Delta f. \tag{7}$$

This noise, which sums with that of the thermal noise due to the feedforward amplifier (5), has a spectrum that is flat for frequencies below the high-pass pole of the recording preamplifier and falls off with a first order slope for higher frequencies. Assuming the real pole approximation of (2), the resulting input referred thermal noise (in the neural signal bandwidth of 30 Hz–3 kHz) is

$$\overline{v_{\rm ni}^2} = \frac{(C_{\rm F}+C_{\rm I})^2}{C_{\rm I}^2}\frac{16kT}{3g_m}(3\,{\rm kHz}-30\,{\rm Hz}) + \frac{C_{\rm F}}{C_{\rm I}^2}\frac{16kT}{3\pi}\left[\frac{f_{\rm HP}}{f_{\rm HP}+30{\rm Hz}}-\frac{f_{\rm HP}}{f_{\rm HP}+3\,{\rm kHz}}\right]. \quad (8)$$

Setting a very low cutoff frequency results in a high level of spot noise at frequencies below the high-pass cutoff frequency. In the pass-band, the noise from the feedback amplifier appears qualitatively similar to $1/f$ noise on top of the thermal noise of the main amplifier, as observation of the flat noise level at low frequencies requires slow measurements. True $1/f$ noise in the system and measurement setup can prevent observation of the flat, low-frequency spectrum.

It is intuitively attractive to assume that tuning of the high-pass cutoff frequency would shape the noise of the feedback amplifier in a manner similar to the gain-bandwidth relationship of a standard feedback amplifier; however, this is not the case. Due to the relationships

$$\sqrt{\overline{v_{\rm no,fb}^2}}\bigg|_{f=0} \propto \sqrt{\frac{1}{g_{\rm mf}}} \quad (9)$$

$$f_{\rm HP} \propto \frac{1}{g_{\rm mf}} \quad (10)$$

a one-decade change in cutoff frequency results in a half-decade change in the RMS noise level at dc. As a consequence of this relationship, a high-pass cutoff frequency at a very low frequency results in minimal noise in the bandwidth relevant to neural action potentials, despite the high noise levels at low frequencies. The need to minimize noise in the bandwidth relevant to neural signals (30 Hz–3 kHz) places an upper limit on the high pass cutoff frequency, so that the filtering is best suited for removing low-frequency electrochemical offsets from the electrode. The data acquisition system must provide an additional high-pass filter to remove out-of-band signals.

Although frequency-shaping techniques may reduce the noise contributions of the feedback amplifier in the neural bandwidth [31], a simpler method is optimization of the feedback capacitors, which reduces the noise contributions from the feedback amplifier. Increasing $C_{\rm F}$ requires a proportional increase in $g_{\rm mf}$ to maintain the same cutoff frequency, resulting in lower output noise, according to (6). Increases in $C_{\rm I}$ must occur with any increase in $C_{\rm F}$; otherwise, the reduction in system gain results in higher input referred noise, as in (8). Alternatively, increasing $C_{\rm I}$ alone increases the gain of the system, providing an area efficient means of reducing the effect of the feedback noise.

2) Stimulation Buffer: The stimulation buffer (Fig. 6 and Table II) uses digital inputs to control the connection of stimulation voltages, provided by an external digital-to-analog converter (DAC), to the electrode. When the enable line is un-asserted, the combinational logic turns off $M_{\rm P10}$ and $M_{\rm P11}$, so that the stimulation output is high impedance. When enabled, the phase input controls whether the pull-up or pull-down is active, and the output stage drives the electrode to $+V_{\rm stim}$ or $-V_{\rm stim}$.

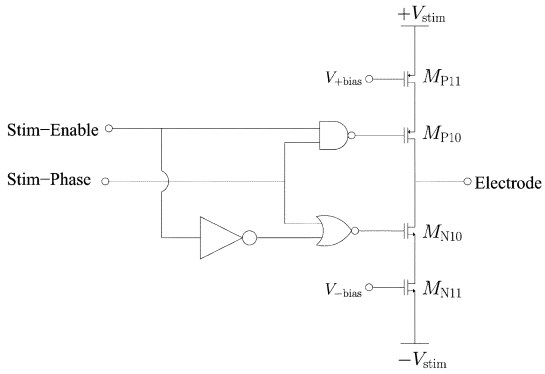

Fig. 6. Schematic of stimulation buffer. When the enable signal is active, the output stage drives the electrode to the positive or negative stimulation voltage, depending on the phase input. The stimulation voltages are generated by a DAC external to the IC. When disabled, the output is high impedance.

TABLE II
TRANSISTOR SIZES IN THE STIMULATION BUFFER

Transistor	Width (μm)	Length (μm)
$M_{\rm P10}$, $M_{\rm P11}$, $M_{\rm P12}$	18.0	1.0
*p*FETs in Logic Gates	6.0	1.0
$M_{\rm N10}$, $M_{\rm N11}$, $M_{\rm N12}$	6.0	1.0
*n*FETs in Logic Gates	2.0	1.0

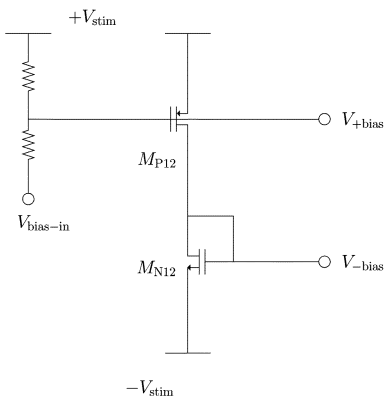

Fig. 7. Bias network that produces $V_{-\rm bias}$ and $V_{+\rm bias}$ from a single voltage input.

The two transistors closest to the stimulation voltages limit the current that the buffer can source or sink into the electrode. The current limits are dependent on both the stimulation voltages and the gate bias voltages on those transistors (see Fig. 7). This dependency does place a minimum voltage requirement on stimulation, as low values of $\pm V_{\rm stim}$ will result in stimulation currents that are insufficient to evoke neuronal activity.

The current limits also govern the transition speed from positive to negative stimulation. For electrode capacitances on the order of 1 nF, the time constant $2c_{\rm e}/g_{m,{\rm out}}$, where $g_{m,{\rm out}}$ is the transconductance of the output stage transistor (either $M_{\rm P10}$ or $M_{\rm P11}$, depending on the polarity of the stimulation), dominates over the relatively quick switching speeds of the logic gates.

TABLE III
AMPLIFIER ACTIVITY DURING OPERATION MODES

Amplifier	Recording	Stimulation	Artifact Elimination
Feed-forward	On	Off	On
Feedback	On	On	On
Stimulation	Off	On	Off
Discharge	Off	Off	On

3) Artifact Elimination: To eliminate the interference with recording after stimulation, commonly referred to as the stimulation artifact, we must discharge the electrode back to the electrochemical offset voltage of the electrode. The feedback capacitors of the recording preamplifier provide the storage elements necessary to track the average electrode voltage. By tracking the average voltage, rather than instantaneous voltage, we minimize interference from neuronal activity that occurs immediately before stimulation on the stored voltage.

To reduce the alteration of the stored charge in the capacitors and to prevent saturation of the rest of the recording signal chain, we must disable the feedforward amplifier. We disable the feedforward amplifier by open circuiting its tail current supply, a method that minimizes charge injection.

After stimulation, we connect a discharge amplifier in a feedback loop with the recording preamplifier. Neglecting the slow effect of the feedback amplifier, the capacitors in the recording preamplifier store the offset voltage of the electrode, such that the output of the recording preamplifier will return to ground when the electrode returns to its pre-stimulation voltage. The feedback loop controls the current output of the discharge amplifier, ensuring that it acts to bring the electrode back to its pre-stimulation voltage. The tail current supply of the discharge amplifier limits the maximum discharge current, preventing unintended neuronal stimulation. This method ensures that the stimulation and artifact elimination currents have no net effect on the electrode charge, although the use of charge balancing on the stimulus signal may still improve artifact elimination duration by minimizing the necessary correction to the electrode voltage that the discharge amplifier must make. For a summary of the activity of the different amplifiers during stimulation and artifact elimination, please see Table III.

During the discharge phase, the discharge amplifier and recording preamplifier function in a closed loop, as shown in Fig. 8. Because there are multiple poles in the discharge path, there is a possibility of unstable loop dynamics. Investigating stability requires identification of the open-loop poles and zeros, as well as the loop gain. In addition to the poles and zeros from the recording preamplifier (2)–(4), the discharge amplifier and a polarizable electrode introduce a pole

$$p_{\mathrm{d}} = -\frac{1}{r_{\mathrm{s}} C_{\mathrm{I}}} \tag{11}$$

and a zero

$$z_{\mathrm{d}} = -\frac{1}{r_{\mathrm{s}} c_{\mathrm{e}}} \tag{12}$$

where r_{s} is the spreading resistance of the electrode, and c_{e} is the electrode interface capacitance. Assuming typical electrode parameters of $r_{\mathrm{s}} = 10\,\mathrm{k}\Omega$ and $c_{\mathrm{e}} = 3\,\mathrm{nF}$, we have $|p_{\mathrm{d}}| = 8\,\mathrm{MHz}$ and $|z_{\mathrm{d}}| = 2.6\,\mathrm{kHz}$. The discharge system also introduces a pole

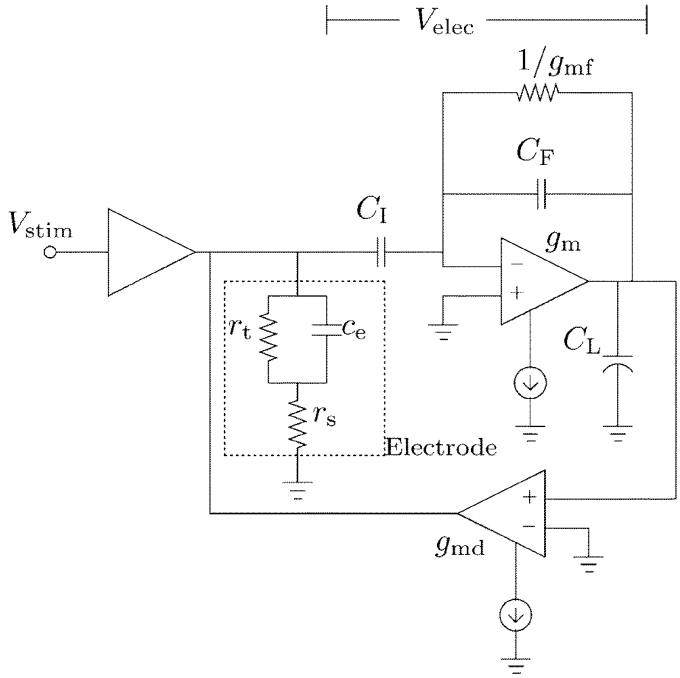

Fig. 8. Complete recording, stimulation, and artifact elimination system. During the discharge phase, the capacitors in the recording system store the electrode offset voltage, V_{elec}.

at the origin that cancels out the zero of the bandpass recording preamplifier.

The loop gain consists of the product of the recording system gain and the gain of the discharge amplifier,

$$A_{\mathrm{disch}} = g_{\mathrm{md}}[r_{\mathrm{out}} \,||\, (r_{\mathrm{t}} + r_{\mathrm{s}})] \tag{13}$$

where r_{out} is the output resistance of the discharge amplifier.

Increasing the bias current of the discharge amplifier increases the loop gain, affecting the system in two ways. First, the slow pole from the high-pass filter moves towards the zero from the electrode and spreading resistance, increasing the speed of the system response. The time constant of that electrode zero sets the limiting speed for discharge, so that less capacitive electrodes will discharge faster. Second, the poles from the low pass recording response and the discharge system meet, branch off from the real axis, and move toward the RHP zero. For large loop gains, these complex poles cause system instability. A loop gain of 100 000 yields a 45° phase margin (see Fig. 9). At this gain, the dominant pole, originally from the high-pass filter, has moved almost to the electrode zero. Further increases to the loop gain increase the overshoot, eventually leading to instability, without significantly improving the linear behavior of the discharge. In practice, slew-rate limiting occurs during discharge, so that there is some performance improvement for larger discharge currents.

Separating the recording and discharge poles will increase the stability margin. This requires lowering the recording pole or increasing the discharge pole. The recording pole must remain above 10 kHz, or attenuation of action potentials will occur. The remaining method to increase the stability margin is to speed up the discharge pole, which will occur through using a small

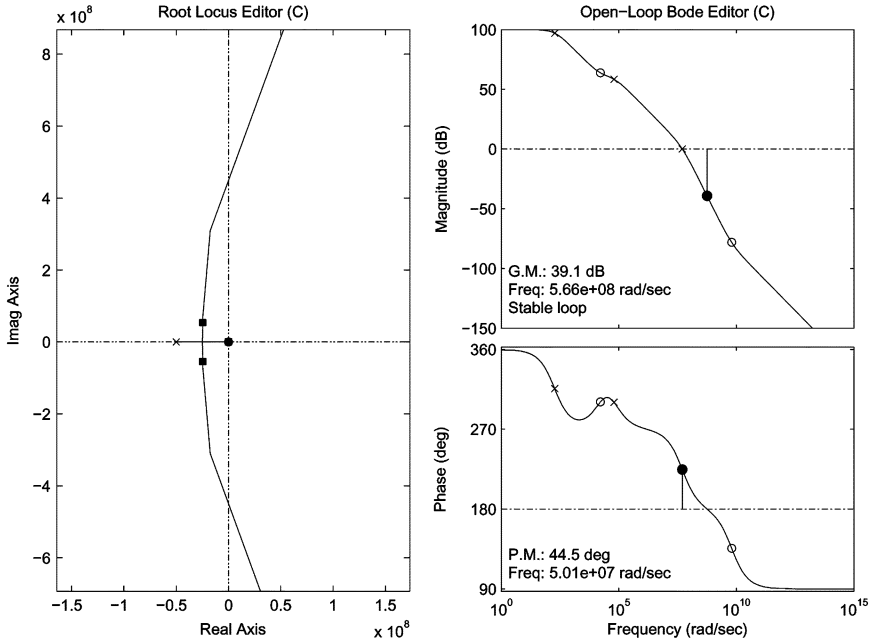

Fig. 9. Theoretical analysis of the discharge loop stability, assuming typical electrode parameters of $r_{\mathrm{s}} = 10$ kΩ and $c_{\mathrm{e}} = 3$ nF. The root locus plot (left) shows the closed loop poles for a 45° phase margin, which occurs for a closed loop gain of 100 000. The bode plots show the magnitude (top right) and phase (bottom right) response for the open loop.

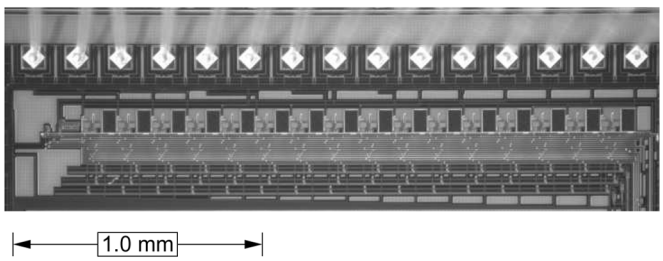

Fig. 10. Die photograph showing the area of active circuitry for 16 stimulation and recording channels.

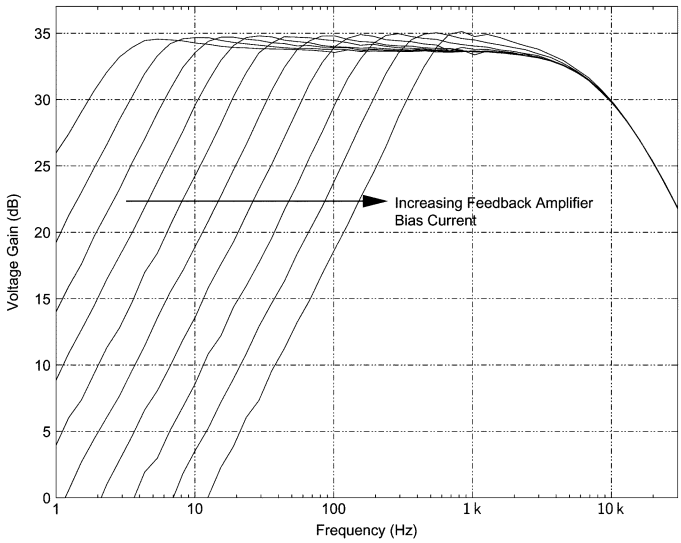

Fig. 11. Frequency response of the recording system. The different high pass poles are the result of 50-mV increments in the feedback bias voltage. The equal frequency spacing is a consequence of the feedback amplifier's operating in weak inversion (subthreshold).

value of C_{I}. The stability requirements of moderate loop gain and small input capacitance are in direct opposition to those for minimizing the effect of noise from the feedback amplifier. The combination of our recording gain of 50 and the maximum discharge gain of 130 ($g_{\mathrm{md}} \approx 85\ \mu\mathrm{S}, r_{\mathrm{out}} \approx 1.6$ MΩ) is a loop gain of 6500, which leaves a large gain margin.

III. Experimental Characterization

We have fabricated the design using the Taiwan Semiconductor Manufacturing Company 0.35-μm process (Fig. 10), available through the MOSIS service. The stimulation and recording circuitry for a single electrode occupies 140 μm $\times$ 230 μm (not including digital control). The die includes circuitry for 16 electrode channels. Our test setup included the IC, a microcontroller (PIC18LF452) to control the stimulation and artifact-elimination timing, external DACs to set the stimulation bias voltages (DAC8420), and additional off-chip amplifiers (LF347) that brought the total recording gain up to 1800 (65 dB).

A. Recording

Evaluating the capabilities of the recording preamplifier consisted of measuring its frequency response (Fig. 11) and input noise (Fig. 12). We measured a midband gain of 48.1 (33.6 dB), which fell slightly short of the design goal of 50. The experiments confirmed that adjusting the bias voltage of the feedback amplifier effectively controlled the high pass pole over a range of 2 Hz $< f_{\mathrm{HP}} <$ 300 Hz. For power supplies of $V_{\mathrm{DD}} = 2.0$ V and $V_{\mathrm{SS}} = -1.8$ V, the power consumption was 100 μW per amplifier.

The location of the high-pass pole strongly affected the overall system noise, as (8) predicted. Low values of the

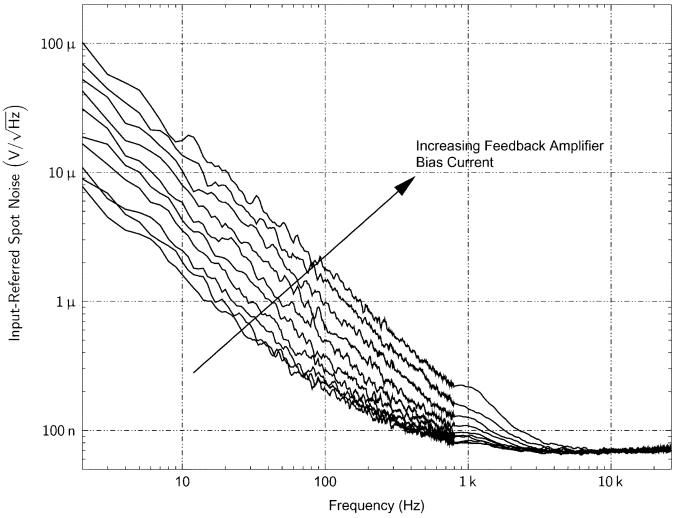

Fig. 12. Input referred noise of the recording system. As the bias current of the feedback amplifier increases, the high-pass cutoff frequency and the amount of noise in the neural bandwidth of 3–30 kHz both increase.

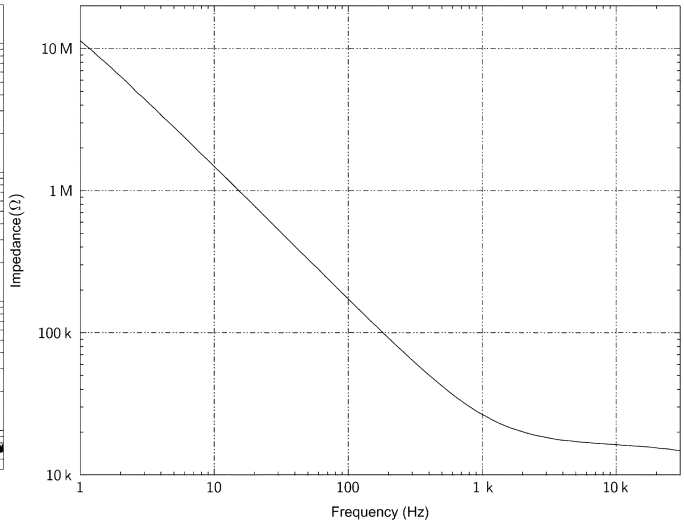

Fig. 13. Frequency impedance plot of the electrode.

TABLE IV
SUMMARY OF INPUT REFERRED NOISE (30 Hz–3 kHz)
($C_{\rm I} = 2$ pF, $C_{\rm F} = 40$ fF, $I_{\rm T} = 13$ μA)

$f_{\rm HP}$ (Hz)	Predicted Noise ($\mu {\rm V}_{\rm rms}$)	Measured Noise ($\mu {\rm V}_{\rm rms}$)	Measured NEF
2	1.67	4.77	17.6
4	2.21	4.84	17.9
12	3.50	5.36	20.0
36	5.21	7.32	27.4
116	6.98	12.3	46.1

high-pass control voltage, corresponding to high cutoff frequencies, introduced large amounts of noise into the bandwidth of neural signals. The curves for high values of the control voltage did not reach a flat level at low frequencies, indicating the presence of significant $1/f$ noise in addition to the thermal noise.

An important measure in evaluating the noise performance for an amplifier it its noise efficiency factor (NEF), which compares the noise level with that of a single bipolar transistor consuming the same power and having no excess or $1/f$ noise [32]. The definition of the NEF is

$$\mathrm{NEF} = \sqrt{\frac{\overline{v_{\rm ni}^2} \cdot 2 I_{\rm total}}{\pi \cdot U_{\rm T} \cdot 4kT \cdot \mathrm{BW}}}. \tag{14}$$

Ideally, the NEF is unity; all practical circuits have a higher value. Table IV summarizes the noise and NEF in the relevant neural bandwidth of 30 Hz–3 kHz. There were two significant sources for the discrepancy between predicted and measured noise. First, the predictions neglected the contributions of $1/f$ noise, which dominated for very low cutoff frequencies. Second, the inaccuracies in the assumption of real poles, as in (2), became more significant for faster high-pass cutoffs.

B. Stimulation

The choice of electrode plays an important role in the performance of the stimulation and artifact-elimination circuitry. We chose a commercially available array consisting of 30 μm diameter gold electrodes (Ayanda Biosystems), upon which we have deposited platinum black [33], [34]. Before connecting the MEA to the stimulation and recording system, we characterized the electrode impedance by comparing the voltage drops across the electrode and a known series resistor (Fig. 13). The electrode had an impedance of 30 kΩ at 1 kHz.

The MEA culture dish contained a saline medium formulated to emulate *in vivo* conditions (Hank's Balanced Salt Solution, Hyclone), although no neuronal cells were present. This setup mimicked the electrical conditions present during electrophysiology experiments without the burden of maintaining environmental controls for cell survival.

Using the stimulation buffer, we applied a biphasic voltage pulse, consisting of a 250-μs positive voltage followed by a negative voltage of equal duration, to the electrode. As a consequence of the design of the bias network of the stimulation buffer (see Fig. 7), the maximum available stimulation current depended on the stimulation voltages. To generate enough source-to-gate voltage on $M_{\rm P12}$ to be able to provide approximately 10 μA, we required $+V_{\rm stim} = V_{\rm DD}$. To prevent electrochemical damage that this large voltage might cause, we limited the maximum voltage at the electrode with a 1N4148 diode external to the IC. The negative phase amplitude was $-V_{\rm stim} = 0.5$ V.

Measuring the voltage across a small resistor in series with the electrode allowed us to determine the current provided during stimulation. The additional components (diode, resistor, and an INA129P instrumentation amplifier) necessary for this experiment did add parasitics that may have been of the order of the electrode impedance, thus possibly affecting the results. The diode in parallel to the electrode also may have introduced asymmetry in the current response. The stimulation current (Fig. 14) was consistent with a current-limited voltage source. The peak current provided by the stimulation was approximately 9 μA, enough to evoke neuronal activity [22].

C. Artifact Elimination

For testing the artifact-elimination circuitry, we used the same electrode and setup, including the external diode, as in

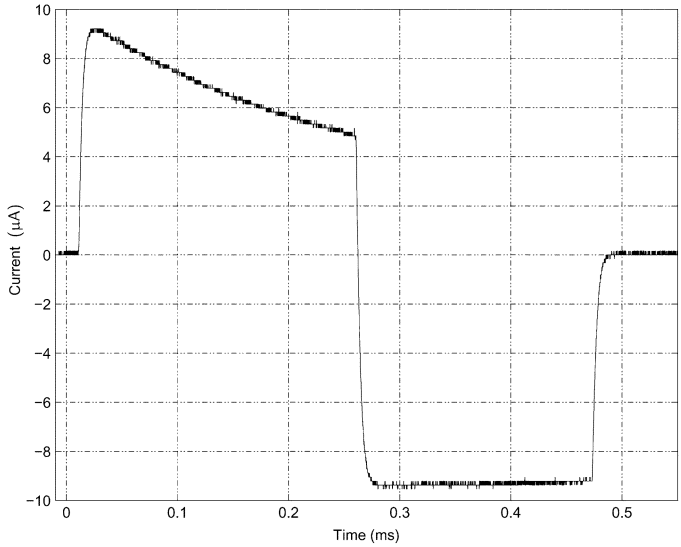

Fig. 14. Current provided by the stimulation buffer. The stimulation buffer was able to provide approximately 9 μA to the electrode.

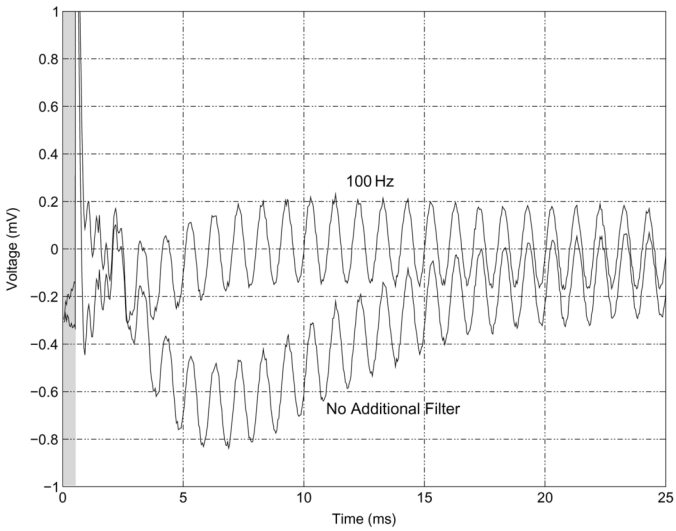

Fig. 16. Effect of a 100-Hz high-pass filter on the artifact remaining after a 1.0-ms discharge. The preamplifier itself contributes a HPF of 21 Hz. A 500-$\mu V_{\rm peak}$, 1-kHz sine wave was present in the saline solution.

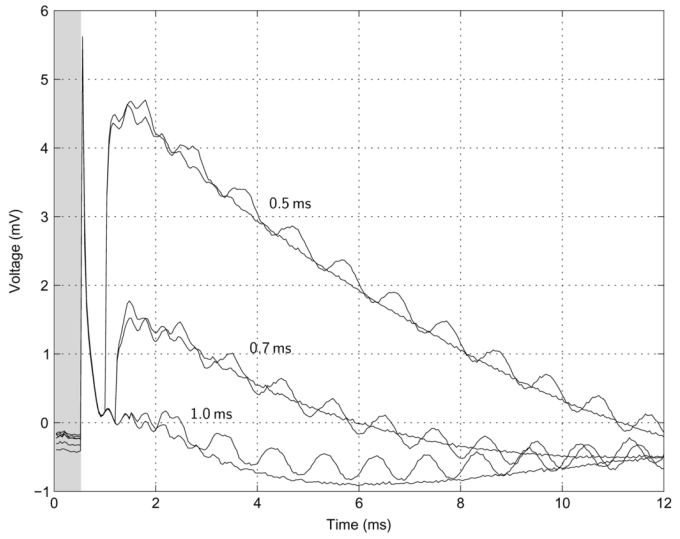

Fig. 15. Effect of the artifact-elimination circuitry. The curves shown are for discharge durations of 0.5, 0.7, and 1.0 ms. Two sets of curves are shown: with and without a 500-$\mu V_{\rm peak}$, 1-kHz sine wave applied to the saline solution. During stimulation, the recording preamplifier is inactive, and the recording in this duration (shaded interval) is due to parasitic coupling through the preamplifier. After stimulation, the artifact-elimination circuitry allows for observation of the sine wave within 2 ms. Without use of the artifact-elimination circuitry, the recording system was saturated for over 15 ms.

Section III-B. We observed the artifact behavior for discharge periods of 0.5, 0.7, and 1.0 ms (Fig. 15). The stimulation parameters were similar to those used during the stimulus current characterization; however, the duration of the negative phase was reduced to 150 μs, resulting in improved charge balance. We set the high-pass cutoff frequency for the preamplifier to 21 Hz, minimizing the thermal noise contributions and the effect of filtering on the artifacts.

Under these stimulation conditions, the stimulation artifact saturated the recording system for over 15 ms. The use of the artifact-elimination circuitry was able to reduce the duration during which the recording system was unusable (Fig. 15). The duration of the discharge played a critical role in the artifact-elimination. For the 0.5-ms discharge, the electrode had not returned to baseline before the end of discharge, resulting in large remaining artifacts. The size of the artifact remaining after discharge decreased with increasing discharge duration; however, we observed an artifact size for 1.0 ms that did not decrease significantly for longer durations.

To demonstrate the effectiveness of the recording system after stimulation, we repeated the stimulation and artifact-elimination trials while applying a 500-$\mu V_{\rm peak}$, 1-kHz sine wave to the saline solution. For all the discharge durations tested, the sine wave was visible within 2 ms of the end of stimulation. The ringing observed after the end of stimulation was likely due to an off-chip amplifier, as the duration of the ringing was independent of the duration of the discharge phase.

Additional reduction of the remaining artifact was possible using an external, first-order high-pass filter (Fig. 16). A 100 Hz filter, which is commonly used for extracellular recordings, attenuated the remaining transient to less than $\pm 250\ \mu$V. (Fig. 16). Although similar results were possible with the filter inherent to the preamplifier, such use would have resulted in a higher level of thermal noise, according to (8).

IV. Discussion and Conclusion

We have presented an analog VLSI system for extracellular stimulation and recording. The design is scalable to MEA systems consisting of thousands of electrodes. A novel feature of the system was the artifact-elimination circuitry, which permitted near-simultaneous stimulation and recording at the same electrode. Results from experimental characterization with a commercial MEA validated the functionality of the electronics.

The recording preamplifier provided an inverting gain of 47.9 and exhibited a noise level that was dependent on the setting of the high pass pole. Experimental characterization measured input noise levels as low as 4.77 $\mu V_{\rm rms}$ in the bandwidth relevant to neural action potentials. Reduction of the noise levels

from the feedback amplifier (the dominant noise source) would have required the use of larger capacitors at the expense of die area. Alteration of the capacitor ratio, thus increasing the gain, would have greatly decreased the noise contributions of the feedback amplifier; however, there would have been a reduction in the stability margin of the artifact-elimination circuitry. Alternative high-pass topologies could also have resulted in lower noise levels. Reduction of the noise introduced by the feedforward amplifier would have required increasing its bias current, although large current increases would have required commensurate increases in die area to maintain the transistor inversion levels. Our desire to integrate the circuitry for 64 or more electrodes onto a single die demands limited per channel area and power requirements. Our choices of bias levels and capacitor sizes were a balance among noise, stability, power, and area.

The stimulus buffer was capable of delivering voltage stimulation with peak currents of 9 μA, enough to elicit neural activity in many cases; however, some cultures, especially those sparsely plated, may require more current. This current limit was a consequence of the bias network for the stimulus buffer, not of the topology of the buffer itself.

Discharge of the stimulation electrode enabled use of the recording preamplifiers within 2 ms after the end of stimulation at the *stimulation* electrode. This time is sufficient to observe responses to stimulation in many experimental situations. The system remained stable, even under a strong discharge amplifier bias.

Future efforts are underway on two fronts: biological validation and improved circuit development. Although the use of saline medium only facilitated the characterization of the electronics, adding neural cell culture to the saline medium is necessary for evaluation of the capability to stimulate the neurons and to record evoked potentials. Verification of the biological interface is necessary to prepare the system for use in scientific studies.

Among the potential improvements to the system, the most important are lower noise levels, more flexible and effective stimulation, and simplified interfacing to computer analog-to-digital converter systems. The simplest method to reduce the noise levels is to increase the feedback capacitors, reducing the noise contribution of the feedback amplifier. The limits in the stimulation current are due to the stimulation bias network; a redesigned bias will permit larger currents for stimulation of sparser cultures. A final need in future designs is for reduction of the output pin count. Integration of data converters onto the IC raises the possibility of digital multiplexing to conserve output pins, as well as reducing the complexity of the computer data acquisition system.

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